TECHNIQUES FOR HANDLING NOISE AND VARIABILITY IN ANALOG CIRCUITS

ON-LINE CLASS on MS TEAMS

January 20-31, 2025

WEEK 1	**JANUARY 20-24**
WEEK 2	**JANUARY 27-31**

DAILY	Central European Time	Eastern Standard Time	Pacific Standard Time	India Standard Time
	CET (Lausanne)	**EST (New York)**	**PST (California)**	**IST (India)**
Module 1	3:00-4:30 pm	9:00-10:30 am	6:00-7:30 am	7:30-9:00 pm
Module 2	5:00-6:30 pm	11:00 am-12:30 pm	8:00-9:30 am	9:30-11:00 pm

WEEK 1	*Module*		
DAY 1, Mon. January 20	1&2	Random Mismatch Origins	Marcel Pelgrom
DAY 2, Tue. January 21	1&2	Analyzing Mismatch and Yield in Analog Circuits	Marcel Pelgrom
DAY 3, Wed. January 22	1&2	Layout Strategies to Reduce Offset	Marcel Pelgrom
DAY 4, Thu. January 23	1&2	Fundamentals of Noise in Electronic Devices	Christian Enz
DAY 5, Fri. January 24	1	Offset and CMRR: Systematic and Random	Michiel Steyaert
	2	Voltage and Current References	Michiel Steyaert

WEEK 2	*Module*		
DAY 6, Mon. January 27	1	Noise Cancellation Techniques	Filip Tavernier
	2	Noise Sampling in Switched Capacitor Filters	Filip Tavernier
DAY 7, Tue, January 28	1&2	Noise Analysis in Continuous-Time and Sampled-Data Circuits	Christian Enz
DAY 8, Wed. January 29	1	Noise and Offset Reduction Techniques	Christian Enz
	2	Dynamic Offset-Cancellation Techniques	Kofi Makinwa
DAY 9, Thu. January 30	1	Dynamic Offset-Cancellation Techniques	Kofi Makinwa
	2	Dynamic Element Matching Techniques	Kofi Makinwa
DAY 10, Fri. January 31	1	Dynamic Element Matching Techniques	Kofi Makinwa
	2	Case Studies in Precision Analog Circuit Design	Kofi Makinwa