PLL Design

ON-LINE CLASS on Microsoft TEAMS

April 15-26, 2024

WEEK 1	**APRIL 15-19, 2024**
WEEK 2	**APRIL 22-26, 2024**

DAILY	Central European Time	Eastern Standard Time	Pacific Standard Time	India Standard Time
	CET (Lausanne)	**EST (New York)**	**PST (California)**	**IST (India)**
Module 1	3:00-4:30 pm	9:00-10:30 am	6:00-7:30 am	6:30-8:00 pm
Module 2	5:00-6:30 pm	11:00 am-12:30 pm	8:00-9:30 am	8:30-10:00 pm

WEEK 1	***Module***		
Monday, April 15	1	Fundamentals of Analog PLLs	Michiel Steyaert
	2	Interference Effects in PLLs	Michiel Steyaert
Tuesday, April 16	1 & 2	Spiral Inductor Interference, Deadzone and Phase Noise	Michiel Steyaert
Wednesday, April 17	1 & 2	VCO Design	Ali Hajimiri
Thursday, April 18	1 & 2	Jitter and Phase Noise in PLLs	Ai Hajimiri
Friday, April 19	1 & 2	Analog Fractional-N PLLs for Frequency Synthesis	Ian Galton
WEEK 2	***Module***		
Monday, April 22	1 & 2	All-Digital PLL Architecture and Implementation	Bogdan Staszewski
Tuesday, April 23	1	Digitally-Controlled Oscillator (DCO)	Bogdan Staszewski
	2	Time-to-Digital Converter (TDC)	Bogdan Staszewski
Wednesday, April 24	1	PLL Analysis and Modeling	Sam Palermo
	2	FDC-based Digital PLLs	Ian Galton
Thursday, April 25	1	PLL Building Blocks	Sam Palermo
	2	Clock Generation and Distribution in Wireline Systems	Sam Palermo
Friday, April 26	1	PLL-Based Clock and Data Recovery Systems	Sam Palermo