Wireline SERDES Transceivers

ON-LINE CLASS by Microsoft TEAMS

MAY 10-21, 2027

WEEK 1		**MAY 10-14, 2025**
WEEK 2		**MAY 17-21, 2026**

		Central European Time	Eastern Standard Time	Pacific Standard Time	India Standard Time
DAILY		**CET (Lausanne)**	**EST (New York)**	**PST (California)**	**IST (India)**
Module 1		3:00-4:30 pm	09:00-10:30 am	6:00-7:30 am	6:30-8:00 pm
Module 2		5:00-6:30 pm	11:00am -00:30pm	8:00-09:30 am	8:30-10:00 pm
WEEK 1	*Module*				
DAY 1, MON May 10	1	Introduction to Wireline Transceivers			Sam Palermo
	2	Transmitters (CML/VM)			Sam Palermo
DAY 2, TUE May 11	1	FIR Equalizers (Tx/Rx)			Sam Palermo
	2	CTLE			Sam Palermo
DAY 3, WED May 12	1	DFE, adaptation			Sam Palermo
	2	Phase-Locked Loops			Sam Palermo
DAY 4, THU May 13	1	Advanced PLLs			Sam Palermo
	2	Clock and Data Recovery			Sam Palermo
DAY 5, FRI May 14	1	Phase/Frequency detectors			Sam Palermo
	2	Advanced CDRs			Sam Palermo
WEEK 2					
DAY 6, MON May 17	1	Baud-rate CDRs			Sam Palermo
	2	Trans-Impedance Amplifiers			Sam Palermo
DAY 7, TUE May 18	1	Advance Signaling Methods			Armin Tajalli
	2	Short Reach Transceiver Design Tradeoffs			Armin Tajalli
DAY 8, WED May 19	1	Tradeoffs in Design of Slicers			Armin Tajalli
	2	Discrete-Time Front-End Design			Armin Tajalli
DAY 9, THU May 20	1	Optical Transmitters			Sam Palermo
	2	ADC-Based RX Analysis and Digital Equalization			Sam Palermo
DAY 10, FRI May 21	1	Wireline RX Time-Interleaved ADC Design and Calibration			Sam Palermo
	2	DSP-DAC Wireline Transmitters			Sam Palermo