Wireline SERDES Transceivers

ON-LINE CLASS by Microsoft TEAMS

May 12-23, 2025

WEEK 1		**MAY 12-16, 2024**
WEEK 2		**MAY 19-23, 2024**

		Central European Time	Eastern Standard Time	Pacific Standard Time	India Standard Time
DAILY		**CET (Lausanne)**	**EST (New York)**	**PST (California)**	**IST (India)**
Module 1		3:30-5:00 pm	09:30-11:00 am	6:30-8:00 am	7:00-8:30 pm
Module 2		5:30-7:00 pm	11:30am -01:00pm	8:30-10:00 am	9:00-10:30 pm
WEEK 1	*Module*				
DAY 1, MON May 12	1	Introduction to Wireline Transceivers			Pavan Hanumolu
	2	Transmitters (CML/VM)			Pavan Hanumolu
DAY 2, TUE May 13	1	FIR Equalizers (Tx/Rx)			Pavan Hanumolu
	2	CTLE			Pavan Hanumolu
DAY 3, WED May 14	1	DFE, adaptation			Pavan Hanumolu
	2	Phase-Locked Loops			Pavan Hanumolu
DAY 4, THU May 15	1	Advanced PLLs			Pavan Hanumolu
	2	Clock and Data Recovery			Pavan Hanumolu
DAY 5, FRI May 16	1	Phase/Frequency detectors			Pavan Hanumolu
	2	Advanced CDRs			Pavan Hanumolu
WEEK 2					
DAY 6, MON May 19	1	Baud-rate CDRs			Pavan Hanumolu
	2	Trans-Impedance Amplifiers			Pavan Hanumolu
DAY 7, TUE May 20	1	Advance Signaling Methods			Armin Tajalli
	2	Short Reach Transceiver Design Tradeoffs			Armin Tajalli
DAY 8, WED May 21	1	Tradeoffs in Design of Slicers			Armin Tajalli
	2	Discrete-Time Front-End Design			Armin Tajalli
DAY 9, THU May 22	1	Optical Transmitters			Sam Palermo
	2	ADC-Based RX Analysis and Digital Equalization			Sam Palermo
DAY 10, FRI May 23	1	Wireline RX Time-Interleaved ADC Design and Calibration			Sam Palermo
	2	DSP-DAC Wireline Transmitters			Sam Palermo