PLL Design

ON-LINE CLASS by Microsoft TEAMS

March 16-27, 2026

WEEK 1		**March 16-20, 2026**			
WEEK 2		**MARCH 23-27, 2026**			
		Central European Time	Eastern Standard Time	Pacific Standard Time	India Standard Time
DAILY		**CET (Lausanne)**	**EST (New York)**	**PST (California)**	**IST (India)**
Module 1		3:30-5:00 pm	9:30-11:00 am	6:30-8:00 am	7:00-8:30 pm
Module 2		5:30-7:00 pm	11:30 am -1:00 pm	8:30-10:00 am	9:00-10:30 pm
WEEK 1	*Module*				
DAY 1, MON March 16	1	Fundamentals of Analog PLLs			Michiel Steyaert
	2	Interference Effects in PLL's			Michiel Steyaert
DAY 2, TUE March 17	1&2	Spiral Inductor Interference, Deadzone and Phase Noise			Michiel Steyaert
DAY 3, WED March 18	1	PLL Analysis and Modeling			Sam Palermo
	2	PLL Building Blocks			Sam Palermo
DAY 4, THU March 19	1&2	VCO Design			Ali Hajimiri
DAY 5, FRI March 20	1&2	Jitter and Phase Noise in PLLs			Ai Hajimiri
WEEK 2	*Module*				
DAY 6, MON March 23	1&2	Analog Fractional-N PLLs for Frequency Synthesis			Ian Galton
DAY 7, TUE March 24	1	Clock Generation and Distribution in Wireline Systems			Sam Palermo
	2	PLL-Based Clock and Data Recovery Systems			Sam Palermo
DAY 8, WED March 25	1&2	All-Digital PLL Architecture and Implementation			Bogdan Staszewski
DAY 9, THU March 26	1	FDC-based Digital PLLs			Ian Galton
	2	Digitally-Controlled Oscillator (DCO)			Bogdan Staszewski
DAY 10, FRI March 27	1	Time-to-Digital Converter (TDC)			Bogdan Staszewski
	2	Ultra-low noise PLL-Reference Co-design Techniques			Taekwang Jang