Mixed-Signal IC Design

ON-LINE Course using Microsoft TEAMS

OCTOBER 12-23, 2026

WEEK 1	**OCTOBER 12-16**
WEEK 2	**OCTOBER 19-23**

DAILY	Central European Time **CET (Lausanne)**	Eastern Standard Time **EST (New York)**	Pacific Standard Time **PST (California)**	India Standard Time **IST (India)**
Module 1	3:00-4:30 pm	9:00-10:30 am	6:00-7:30 am	7:30-9:00 pm
Module 2	5:00-6:30 pm	11:00 -12:30 pm	8:00-9:30 am	9:30-11:00pm

WEEK 1	Module		
DAY 1, Mon. Oct. 12	1	The Analog-Digital Trade-off - The Impact of Technology Scaling	Jan Rabaey
	2	ULP Mixed-Signal Design for IoT and Weareable Devices: Sensing and Data Acquisition	Jan Rabaey
DAY 2, Tue. Oct. 13	1	ULP Mixed-Signal Design for IoT and Weareable Devices: Communication and Computation	Jan Rabaey
	2	ULP Mixed-Signal Design for IoT and Weareable Devices: Energy Harvesting, Storage and Conversion	Jan Rabaey
DAY 3, Wed. Oct. 14	1	Evolution in Digital CMOS Technology and its Impact on Design	Jan Rabaey
	2	Design Methodolgy for Systems-on-a-Chip	Jan Rabaey
DAY 4, Thu, Oct. 15	1&2	Modeling and Simulation, Design Methodology	Pavan Hanumolu
DAY 5, Fri. Oct. 16	1&2	Time Varying Circuits in Mixed-Signal Design	Shanthi Pavan

WEEK 2	Module		
DAY 6, Mon. Oct. 19	1	Offset and CMRR: Random and Systematic	Michiel Steyaert
	2	Fully-Differential Amplifiers	Michiel Steyaert
DAY 7, Tue. Oct. 20	1	Interference Effects and PSRR	Michiel Steyaert
	2	Circuit Design for EMC	Michiel Steyaert
DAY 8, Wed. Oct. 21	1&2	Noise Coupling in Mixed-Mode ICs: Mechanisms, Simulation, Measurement	Tim Schmerbeck
DAY 9, Thu. Oct. 22	1	Noise Coupling in Mixed-Mode ICs: Design Strategy/Hardware Example	Tim Schmerbeck
	2	Design for (ESD) Robustness in Silicon ICs	Tim Schmerbeck
Day 10, Fri. Oct. 23	1	Practical Techniques of Frequency Compensation	Vadim Ivanov
	2	Power Management in Efficient Mixed-Signal Integrated Systems	Vadim Ivanov