# PLL Design

**Live Course @ EPFL, Lausanne, Switzerland**

**JUNE 19-23, 2023**

## MONDAY, June 19

| | | |
|---|---|---|
| 8:30-10:00 am | Fundamentals of Analog PLLs | Michiel Steyaert |
| 10:30-12:00 am | Interference Effects in PLL's | Michiel Steyaert |
| 1:30-5:00 pm | Spiral Inductor Interference, Deadzone and Phase Noise | Michiel Steyaert |

## TUESDAY, June 20

| | | |
|---|---|---|
| 8:30-12:00 am | VCO Design | Ali Hajimiri |
| 1:30-5:00 pm | Jitter and Phase Noise in PLLs | Ali Hajimiri |

## WEDNESDAY, June 21

| | | |
|---|---|---|
| 8:30-10:00 am | PLL Analysis and Modeling | Sam Palermo |
| 10:30-12:00 am | PLL Building Blocks | Sam Palermo |
| 1:30-3:00 pm | Clock Generation and Distribution in Wireline Systems | Sam Palermo |
| 3:30-5:00 pm | PLL-Based Clock and Data Recovery Systems | Sam Palermo |

## THURSDAY, June 22

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|---|---|---|
| 8:30-12:00 am | Analog Fractional-N PLLs for Frequency Synthesis | Ian Galton |
| 1:30-5:00 pm | All-Digital PLL Architecture and Implementation | Bogdan Staszewski |

## FRIDAY, June 23

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|---|---|---|
| 8:30-10:00 am | Digitally-Controlled Oscillator (DCO) | Bogdan Staszewski |
| 10:30-12:00 am | Time-to-Digital Converter (TDC) | Bogdan Staszewski |
| 1:30-3:00 pm | FDC-based Digital PLLs | Ian Galton |