PLL Design

Live Course @ EPFL, Lausanne, Switzerland

June 23-27, 2025

Monday, June 23		
08:30 - 10:00 am	Fundamentals of Analog PLLs	Michiel Steyaert
10:30 - 12:00 am	Interference effects in PLL's	Michiel Steyaert
01:30 - 05:00 pm	Spiral Inductor Interference, Deadzone and Phase Noise	Michiel Steyaert
Tuesday, June 24		
08:30 - 12:00 am	VCO Design	Ali Hajimiri
01:30 - 05:00 pm	Jitter and Phase Noise in PLLs	Ai Hajimiri
Wednesday, June 25		
08:30 - 12:00 am	Analog Fractional-N PLLs for Frequency Synthesis	Ian Galton
01:30 - 05:00 pm	All-Digital PLL Architecture and Implementation	Bogdan Staszewski
Thursday, June 26		
08:30 - 10:00 am	Digitally-Controlled Oscillator (DCO)	Bogdan Staszewski
10:30 - 12:00 am	Time-to-Digital Converter (TDC)	Bogdan Staszewski
01:30 - 03:00 pm	PLL Analysis and Modeling	Sam Palermo
03:30 - 05:00 pm	FDC-based Digital PLLs	Ian Galton
Friday, June 27		
08:30 - 10:00 am	PLL Building Blocks	Sam Palermo
10:30 - 12:00 am	Clock Generation and Distribution in Wireline Systems	Sam Palermo
01:30 - 03:00 pm	PLL-Based Clock and Data Recovery Systems	Sam Palermo