Integrated System Design in AI Era

Live Course @ EPFL, Lausanne, Switzerland

AUGUST 31- SEPTEMBER 4, 2026

Monday, August 31		
08:30 - 12:00 am	Trends in Digital Design and Design Methodologies	Jan Rabaey (Berkeley)
01:30 - 05:00 pm	New Open-Source HW (Single and Multi-Core) Platforms for AI/ML	Frank K. Gurkaynak (ETHZ)
Tuesday, September 1		
08:30 - 10:00 am	New Accelerator-Based Open-Source Hardware and Co-Design Flows	David Atienza (EPFL)
10:30 - 12:00 am	The Open-Source Hardware Ecosystem: Current State and Future Prospects	Davide Schiavone (OpenHW)
01:30 - 05:00 pm	New Memory Technologies (3D Stacking, Ultra-Low Power, etc.)	Andreas Burg (EPFL)
Wednesday, September 2		
08:30 - 12:00 am	Verification and AI-Boosted Chip Design (ABCD)	Subhasish Mitra (Stanford)
	3D and Monolithic Integration	Subhasish Mitra (Stanford)
01:30 - 05:00 pm	HANDS-ON Developing and Testing Heterogeneous Accelerator-Based Platforms	Miguel Peon (EPFL)
Thursday, September 3		
08:30 - 12:00 am	High-level synthesis for optiman and fast design of digital systems	Giovanni De Micheli (EPFL)
01:30 - 05:00 pm	Design and System technology co-optimization beyond 5nm CMOS	Julien Ryckaert (IMEC)
Friday, September 4		
08:30 - 12:00 am	Evolving and Open-Source Architectures	Abbas Rahimi (IBM)
01:30 - 03:00 pm	Overview of Various System-Level Industrial Case Studies Designs	David Atienza (EPFL)