Integrated System Design in 5nm Era

Live Course @ EPFL, Lausanne, Switzerland

JANUARY 27-31, 2025

Monday, January 27		
08:30 - 12:00 am	New Nanoscale Technologies and Architectures	Jan Rabaey (Berkeley)
01:30 - 05:00 pm	New Open-Source HW (Single and Multi-Core) Platforms for AI/ML	Frank K. Gurkaynak (ETHZ)
Tuesday, January 28		
08:30 - 10:00 am	New Accelerator-Based Open-Source Hardware and Co-Design Flows	David Atienza (EPFL)
10:30 - 12:00 am	The Open-Source Hardware Ecosystem: Current State and Future Prospects	Davide Schiavone (OpenHW)
01:30 - 05:00 pm	New Memory Technologies (3D Stacking, Ultra-Low Power, etc.)	Andreas Burg (EPFL)
Wednesday, January 29		
08:30 - 12:00 am	Using HLS as New Approach to Speed up Digital System Specification and Design	Nanni De Micheli (EPFL)
01:30 - 05:00 pm	HANDS-ON Developing and Testing Heterogeneous Accelerator-Based Platforms	David Atienza (EPFL)
Thursday, January 30		
08:30 - 12:00 am	3D and Monolithic Integration	Subhasish Mitra (Stanford)
01:30 - 05:00 pm	Design and System technology co-optimization beyond 5nm CMOS	Julien Ryckaert (IMEC)
Friday, January 31		
08:30 - 12:00 am	Neuro-Vector-Symbolic Architectures: An Algorithmic-Hardware Framework Towards Artificial General Intelligence	Abbas Rahimi (IBM)
01:30 - 03:00 pm	Overview of Various System-Level Industrial Case Studies Designs	David Atienza (EPFL)