PRACTICAL DESIGN OF DATA CONVERTERS

ON-LINE CLASS on MS TEAMS

MARCH 10-21 , 2025

WEEK 1	**MARCH 10-14**
WEEK 2	**MARCH 17-21**

DAILY	Central European Time	Eastern Standard Time	Pacific Standard Time	India Standard Time
	CET (Lausanne)	**EST (New York)**	**PST (California)**	**IST (India)**
Module 1	3:00-4:30 pm	9:00-10:30 am	6:00-7:30 am	7:30-9:00 pm
Module 2	5:00-6:30 pm	11:00 am-12:30 pm	8:00-9:30 am	9:30-11:00 pm

WEEK 1	*Module*		
DAY 1, Mon. March 10	1	Specifications Overview: INL, DNL, THD, SFDR, SNR, DR, ENOB, jitter	Marcel Pelgrom
	2	ADC Comparators	Marcel Pelgrom
DAY 2, Tue. March 11	1&2	Basic ADC Topologies: Overview	Marcel Pelgrom
DAY 3, Wed. March 12	1&2	Time Interleaved ADC	Marcel Pelgrom
DAY 4, Thu. March 13	1	Limits of Nyquist ADC Architecture	Filip Tavernier
	2	Case Study of a High-Speed Single-Channel SAR ADC	Filip Tavernier
DAY 5, Fri. March 14	1	Case Study of a Time-Interleaved Hybrid ADC	Filip Tavernier
	2	Oversampling ADCs : Discrete-and-Continuous-time Delta-Sigma Converters	Shanthi Pavan
WEEK 2	*Module*		
DAY 6, Mon. March 17	1	Case Study: Low-Power Data Converters (1)	Kofi Makinwa
	2	Case Study: Low-Power Data Converters (2)	Kofi Makinwa
DAY 7, Tue. March 18	1	Simulating ADCs: Frequency Domain: FFT, Bin Choice, Windowing, Noise Level, kT/C Noise	Shanthi Pavan
	2	Continuous-Time Pipeline ADC	Shanthi Pavan
DAY 8, Wed. March 19	1&2	Current Steering DAC's	Klaas Bult
DAY 9, Thu. March 20	1&2	Mismatch-Shaping Multi-bit DACs	Ian Galton
DAY 10, Fri. March 21	1	Simulating Sigma-Delta Converters	Shanthi Pavan
	2	Case Study: High-Performance Delta-Sigma Converter	Shanthi Pavan