# Practical Aspects of Mixed-Signal IC Design

**ON-LINE CLASS by MS TEAMS**

**AUGUST 30 - SEPTEMBER 10, 2021**

## Week 1

<table>
<thead>
<tr>
<th>Module</th>
<th>Dates</th>
<th>Time CET (Lausanne)</th>
<th>Time EST (New York)</th>
<th>Time PST (California)</th>
<th>Time IST (India)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Module 1</td>
<td>Aug 30-31</td>
<td>4:00-5:30 pm</td>
<td>10:00-11:30 am</td>
<td>7:00-8:30 am</td>
<td>7:30-9:00 pm</td>
</tr>
<tr>
<td>Module 2</td>
<td>Aug 30-31</td>
<td>6:00-7:30 pm</td>
<td>12:00 am-1:30 pm</td>
<td>9:00-10:30 am</td>
<td>9:30-11:00 pm</td>
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### Daily (August 30-31)

- **Monday, August 30**
  1. The Analog-Digital Trade-off - The Impact of Technology Scaling
  2. ULP Mixed-Signal Design for IoT and Biomedical Interfaces

- **Tuesday, August 31**
  1. ULP Mixed-Signal Design for IoT and Biomedical Interfaces

### DAILY (September 1-10)

- **Wednesday, Sept 1**
  1. Offset and CMRR: Random and Systematic
  2. Fully-Differential Amplifiers

- **Thursday, Sept 2**
  1. Interference Effects: CMRR/PSRR
  2. Circuit Design for EMC

- **Friday, Sept 3**
  1. Noise Calculation and Simulation in SC & CT ICs
  2. Noise and Offset Reduction Techniques

## Week 2

<table>
<thead>
<tr>
<th>Module</th>
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</thead>
<tbody>
<tr>
<td>Module 1</td>
<td>Sept 6-10</td>
<td>5:00-6:30 pm</td>
<td>11:00-12:30 am</td>
<td>8:00-9:30 am</td>
<td>8:30-10:00 pm</td>
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### Week 2 Modules

- **Monday, Sept 6**
  1. Noise Coupling in Mixed-Mode ICs:
  2. Mechanisms, Simulation, Measurement

- **Tuesday, Sept 7**
  1. Design Strategy/Hardware Example
  2. Design for (ESD) Robustness in Silicon ICs

- **Wednesday, Sept 8**
  1. Matching Impairments in Mixed-Mode ICs

- **Thursday, Sept 9**
  1. Modeling and Simulation, Design Methodology
  2. Practical Techniques of Frequency Compensation

- **Friday, Sept 10**
  1. Circuit Techniques for OpAmp Speed and Accuracy